#14705, DD4 5-21-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JC675 U.S. PTO 10/020314 12/18/01

In re U.S. Patent Application of	)
SHIMAMOTO et al.	)
Application Number: To Be Assigned	)
Filed: Concurrently Herewith	)
For: FABRICATING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUITS	)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

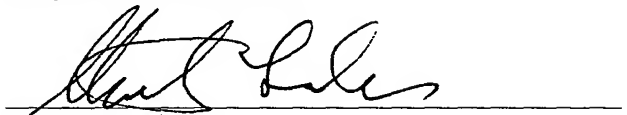
Pursuant to 37 C.F.R. §§ 1.56 and 1.97, this Information Disclosure Statement is submitted in the above-identified patent application. A listing of documents to be published on the face of any patent granted from this application is submitted herewith on Form PTO-1449. Any other documents or information submitted for consideration by the Examiner are listed in this paper. A copy of each U.S. and foreign patent, or each publication or portion thereof listed or herein identified, is submitted herewith.

This Information Disclosure Statement is submitted with the initial application. Accordingly, no fee is due or payable at this time.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Please charge any additional fees or credit any overpayments in connection with this paper to Deposit Account No. 08-1480.

Respectfully submitted,



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